Graig Zethner

Experienced professional with 22+ years of FPGA/ASIC design and verification expertise; owner of three patents. Lead on multiple projects that moved from concept through production. Track record for completing projects successfully and ahead of schedule, as well as implementing new project methodologies to save time and get the product to the end-user as soon as possible. MBA from top-tier University, September 2011.

EDUCATION

New York University – Leonard N. Stern School of Business, New York, New York September 2011
Master of Business Administration Candidate - September 2011

- GPA: 3.85
- Jay S. Wyner Award Recipient, Harold Goldberg Scholar, Stern Scholar, Beta Gamma Sigma Honor Society, Graduate with Distinction
- Specializations: Management of Technology & Operations, Finance
- Courses Include: Outsourcing, High Tech Marketing, Search & The New Economy, Corporate Finance, Valuation, Mergers & Acquisitions, Futures & Options, Statistics, Strategy I, Strategy II, Implementing Strategy, Accounting, Economics, Leadership, Negotiations

Polytechnic University, Farmingdale, New York May 2001
Bachelor of Science and Master of Science, Computer Engineering - Magna Cum Laude

- GPA: 3.93
- Eta Kappa Nu Electrical Engineering Honor Society

SUMMARY

- Experience – 22+ Years of FPGA & ASIC Architecture, Design & Verification
- Design – Architecture, ASIC RTL, FPGA RTL, & Schematic Capture Design
- Verification – Testbench & Sim Creation, Code & Functional Coverage, SVA Formal Verification
- Back End – Synthesis, Timing Closure, Scan Chain & BIST Insertion, Formal Verification
- Production Testing – Functional Test Creation for ATE & Debug with Test Engineers
- Management – Project Manager on several projects, ATE test programs, and ASIC respins
- Awards – Eight-time Qualstar recipient, multiple patents on low-power, high-performance serial link

SKILLS

- Hardware Language: Verilog, System Verilog (including SVA), VHDL, Vera
- Programming: Python, Perl, UNIX Scripting, PHP, MySQL, Javascript, HTML, C, C++, R
- Bus Standards: AXI, AXI-Streaming, AHB, APB, USB, JTAG, DDR, PCI, LPC, SPI, I2C
- Interfaces: 10M/100M/1G/40G/100G Ethernet MII/XAUI/XLAUI, Interlaken, SRIO
- Simulation: IUS, Modelsim, VCS, Novas, Jasper, 0-in CDC
- Backend: Vivado, Design Compiler, Synplicity, Primetime, PTPX, Formality, Spyglass
- Platforms: Windows (XP, Vista, 7, 8.1, 10), MacOS, Linux, Unix
- Other Software: Excel, Word, Powerpoint, Visio, Git, Perforce, Clearcase, CVS, JIRA

EXPERIENCE

Qualcomm Inc., QCT Division, San Diego, California **October 2011 – Present**
Principal Engineer / Manager

- **5G CSM**
  - Designed and implemented 32-core ORAN C-Plane packet processor module, including all interfacing to load balance and offload beamweights to a central codebook.
  - Devised innovative solutions to arbitrate between cores and avoid corruption.
  - Created multiple custom co-processors to accelerate depacketization.
  - Created test-platform for CSM in Ultrascale+ VU13P FPGAs. Custom cores include 100G custom traffic flow generators, 100G hardware-based capture & player cores, and Cortex packet engines.

- **Nomad/Oneweb User Terminal**
  - Managed Rx and Tx data-path integration, register generation, debug feature set, gate-level testing, clock domain crossing checks (CDC), and Lint cleanup prior to release of IP.
  - Designed and verified multiple FIR and IIR blocks for use in DC and Notch filters.

- **MDM/MSM Modem Family (MDM9x25 through MDM9x68 Modems)**
  - Architected, designed, and verified new inter-chip high-speed serial link for low-power, high performance operation. Multiple patents issued.
  - Worked with San Diego, Irvine, and Santa Clara teams to manage updates of Vector Processing Engine and sub-system, including design & power improvements and increased modularity of code.
  - IP, implementation, and synthesis experience with Xilinx UltraScale+, Kintex, and Virtex FPGAs.
  - Experienced in usage of various Xilinx IPs, including Interlaken, CMAC, SRIO, & AXIS cores.

SMSC, Connectivity Solutions Product Group, Hauppauge, New York **January 2009 – September 2011**
Senior Design Engineer

- **USB3 Hub Family, USB3 Graphics Family, Gigabit Ethernet Family**
  - Created DDR2 controller, hextile processor, and AXI/APB bus switches, masters, and slaves.
  - Created Windows 7 targeted wake-on-LAN logic and transmit offload engine.
  - Created & implemented new production test flow which allows complete debug of a test program before silicon arrives, reducing production test development and time to market.

Qualcomm Inc., CRD Division, San Diego, California **March 2007 – January 2009**
Senior Engineer

- **CSM6850 Cell Station Modem**
  - Created and debugged all functional test patterns for test engineers.
  - Created numerous Perl scripts to allow more efficient project management.
  - Designed monitors to check features including interface speeds, memory refresh, and arbitration.

SMSC, NPG Product Group, Hauppauge, New York **April 2001 – February 2007**
Senior Verification Engineer

- **Media Controller Family, Ethernet MAC+PHY Family, Advanced I/O Family**
  - Architected, designed, and verified many blocks for Ethernet-based projects.

ADDITIONAL

- Jeopardy Contestant – Season 27 – March 2011
- Masterminds Winner – Season 4 – September 2023
- Member of American Mensa, Ltd. – October 2008 – Present